

REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 55 and 57-65 are pending; Claims 55 and 57-59 are currently amended; Claims 60-65 are newly added; Claims 1-54 and 56 are canceled.

Response to Double Patenting

Reconsideration of Claims 55-59 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 53, 58, 59 and 67 of copending Application No. 10/935,451 is requested based on the following remarks.

Claim 55 is amended with the limitation that "a solder metal is bonded to a pad with a sidewall not covered by a solder mask", which is not disclosed in copending Application No. 10/935,451. Withdrawal of the provisional rejection to Claims 56-59 on the ground of nonstatutory obviousness-type double patenting is respectfully requested.

Reconsideration of Claims 55-59 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 1-10 of copending Application No. 11/389,717 is requested based on the following remarks.

A terminal disclaimer in compliance with 37 CFR 1.321(c) is submitted. Withdrawal of the rejection to Claims 55-59 under double patenting is respectfully requested.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 55-65

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As currently amended, independent Claim 55 is recited below:

55. A chip package, comprising:
 - a semiconductor device;
 - a substrate comprising a first pad with a sidewall not covered by a solder mask,
 - a metal pillar between said semiconductor device and said substrate, wherein said metal pillar has a thickness of between 10 and 100 microns;
 - a metal layer between said metal pillar and said substrate, wherein said metal layer has a bottom surface partially covered by said metal pillar and partially not covered by said metal pillar; and
 - a solder metal between said metal layer and said substrate, wherein said solder metal is bonded to said first pad.
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Reconsideration of the rejection of Claims 55 and 58 under 35 U.S.C. 102(b) as being anticipated by Ohuchi et al. (US6,495,916) and of the rejection of Claims 56, 57 and 59 under 35 U.S.C. 103(a) as being unpatentable over Ohuchi et al. is requested based on the following remarks.

Applicants respectfully assert that the chip package claimed in amended claim 55 patently distinguishes over the citation by Ohuchi et al. (US6,495,916).

Ohuchi et al. teach a chip package comprising a semiconductor device 1; a metal pillar 4 over said semiconductor device 1, wherein said metal pillar 4 has a thickness of between 10 and 100 microns; a metal layer 14 over said metal pillar 4, wherein said metal layer 14 has a bottom surface partially covered by said metal pillar and partially not covered by said metal pillar; and a solder metal 7 over said metal layer 14. ~
See Fig. 7, lines 3-6, col. 3 and lines 31-36 col. 6 ~

However, Ohuchi et al. fail to teach that said solder metal 7 may be bonded to a pad with a sidewall not covered by a solder mask, as claimed in amended claim 55.

For at least the foregoing reasons, applicants respectfully submit independent Claim 55 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 57-65 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Zarneke not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,



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